PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: LARRY ZHAO JEREMY MARTIN HARTMUT RUELKE	Confirmation No.: 7303 Examiner: Alexander G. Ghyka
Serial No.: 10/717,122	Group Art Unit: 2812
Filed: November 19, 2003	Att'y Docket: 2000.106900/DE0130
For: DIELECTRIC BARRIER LAYER FOR A COPPER METALLIZATION LAYER HAVING A VARYING SILICON CONCENTRATION ALONG ITS THICKNESS	Customer No.: 23720

DECLARATION UNDER 37 C.F.R. § 1.131 HARTMUT RUELKE

1. My name is Hartmut Ruelke. I have personal knowledge of the facts stated herein. I am currently employed with Advanced Micro Devices, Inc. I am a named inventor on U.S. patent application Serial No. 10/717,122 entitled "Dielectric Barrier Layer for a Copper Metallization Layer Having a Varying Silicon Concentration Along Its Thickness."

2. Attached as Exhibit A is a copy of the invention disclosure form that the named inventors prepared for the invention described in the above-referenced U.S. patent application. We prepared and signed the invention disclosure form on April 4 and April 19, 2001, as indicated by the date adjacent each of the signatures.

3. The attached invention disclosure form (Exhibit A) was provided with internal tracking number DE0130 by AMD's legal department, and it was sent to the law firm of Grunecker, Kinkeldey Stockmair & Schwanhausser with a request to prepare a German patent application for the invention disclosed in the invention disclosure form.

4. That German application (Serial No. 103 03 925.2) entitled "A Dielectric Barrier Layer for a Copper Metallization Layer Having a Varying Silicon Concentration Along Its Thickness" was prepared and filed in Germany on January 31, 2003. Exhibit B.

5. I understand that willful false statements and the like so made are punishable by fine or imprisonment, or both, and may jeopardize the validity of the application or any patent issuing thereon.

6. I declare under penalty of perjury that the foregoing is true and correct.

12/10/07
Date

Hartmut Ruelke

EXHIBIT A

AMD INVENTION DISCLOSURE

TLD ID# DE 0130 Rec'd date 04/23/01
Sunnyvale x42110, return to MS68, Texas x55964 return to MS562

Project: ☐, **Product:** ☐, **Process:** ☒, **Technology** ☒, **to which the invention applies (*identify*):** HIP8, HiP9

List 2 to 5 key words useful to search by to find patents or art related to this invention: ____ Copper inlaid lines, reliability, Silicon nitride, interface

Working title of invention: Using a new Cu capping integration to optimize integrated circuit reliability

Inventor's signature : _____ date : 4/9/01
Co-Inventor's printed full name:__Larry Zhao_____ Citizenship:_____P.R.China_____
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Co-Inventor's signature : _____ date : 04 / 19 /01
Co-Inventor's printed full name: Hartmut Ruelke_ Citizenship:__Germany_____
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List on additional sheet if there are more co-inventors and list total number of inventors here:__3_

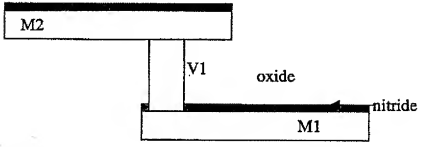
Name(s) of attorney(s) preferred by inventor(s) to prepare patent application, if known: _____
John Hankins @ McDermott, Will and Emery._____ _____

Witness 1 initial: _____ Witness 2 initial: _____

Identify known relevant art (patents, publications, products): _____
_____none.

State the problem solved by this invention:

The current Copper damascene technology has metal-via integration as shown in the following schematic. A lower level metal (called M1 in this disclosure) is connected to an upper level metal (called M2 in this disclosure) through a via (called V1). The metal lines are composed of Copper that is enclosed on all sides by other materials. At the bottom and sides of Copper lines a thin barrier of a different metal such as Tantalum is used. On the top of the Copper lines a dielectric barrier such as silicon nitride (SiN) is used. These barriers are required to serve two critical functions. First, they prevent copper from diffusing through the dielectric material leading to a degradation of the insulating properties of the dielectric and otherwise interfering with the performance of the device. And second, they form a high quality interface with the copper to enhance the electromigration (EM) performance of the Copper line. The present disclosure pertains to the dielectric barrier layer, and particularly to silicon nitride barriers. The present disclosure involves two different deposition processes for SiN, one a more Silicon rich than the other. In this disclosure the Silicon rich SiN will be designated SR-SiN and the other standard SiN film will be designated N-SiN.



EM is a diffusion phenomenon under the influence of electric field. In the Copper damascene structure, Copper diffuses in the direction of flowing electrons, which will eventually produce EM voids in the Copper interconnects and causes device failure. The EM voids typically originate at the Cu/SiN interface, which is one of the most important diffusion paths in Copper damascene structure. Our experiments have shown that the interface of Cu and N-SiN results in better EM performance than Cu and SR-SiN.

It is important for the SiN to function as a Cu diffusion barrier, in that it must prevent Cu from migrating through the barrier to other dielectric layers. At the same time, as backend dimensions scale smaller, there is a need to reduce the capacitive coupling between metal lines. This requires reducing the overall dielectric constant of the dielectric films used in the backend. SiN has a relatively high dielectric constant of approximately 7 versus 2-4 for low k dielectric films. In order to limit the negative consequences of SiN on the capacitive coupling, it is desirable to use a very thin layer. However, thinning the SiN compromises its diffusion barrier properties. Thus it is necessary to improve the Cu diffusion barrier properties of the SiN film in order to allow it be scaled thinner without causing increased Cu diffusion. Our experiments have shown that SR-SiN is a far superior Cu diffusion barrier to N-SiN, even when comparing a SR-SiN film to an N-SiN film 67% thicker. So the problem is that we need to optimize both EM and Cu diffusion barrier performance, and our experiments suggest that different films are required to accomplish each of these goals.

Brief description and/or sketch of invention *(please attach copies of AMD patent notebook pages, reports or drawings)*:

In this disclosure, we propose to optimize reliability performance in terms of both EM and dielectric breakdown by using a new nitride integration. We propose to deposit a thin N-SiN layer (20 – 100 A) first and then a thicker (200 - 700A) SR-SiN layer on top of that. We propose the thickness of N-SiN is about 50A. But the exact thickness of this first layer will depend upon the specific tools and circumstances used in the actual implantation of the invention. What is required is that the N-SiN form a high quality interface with Cu to enhance EM performance.

The deposition of the first SiN layer (N-SIN type film) could be preceded by a plasma treatment of the Cu to remove Cu oxide, such as a reducing treatment such as NH3 and or H2 diluted as needed in N2 or other inert gasses. This will further enhance the electromigration properties of the Cu-SiN interface.

The deposition of the second SiN layer (SR-SiN type film) can be done as an in-situ PE-CVD deposition without a vacuum break. So for example, following the deposition step of the N-SiN film, the RF power would be turned off, the gas flows and other process parameters readjusted to those appropriate for the SR-SiN deposition, and then the RF power restored at an appropriate level to initiate deposition of the SR-SiN.

It may also be possible to transitions the gas flows, RF power levels and other process parameters without turning off the power and ceasing the deposition. In this case the two films would be graded with a finite transition region, rather than an abrupt interface.

In this integration scheme, the Cu/SiN interface will be formed with the N-SiN, while the bulk of the SiN will be composed of the SR-SiN film. Therefore, EM performance will not be compromised since it strongly depends on the Cu/nitride interface property. At same time, the majority of the capping layer is UT PEN. This will still provide excellent resistance to copper diffusion.

Attached are process recipes of the single SiN recipes for 1.) N-SiN and 2.) SR-SiN and 3.) the newly developed integrated two step SiN deposition of the present invention disclosure.

Patent notebook # _____ Page numbers_____ Number of drawings_____

AMD INVENTION DISCLOSURE

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Advantages (check all that apply):

☐ avoids existing patent(s)	☐ improves precision	☐ simplifies manufacturing
X new function	☐ improves accuracy	☐ improves wear characteristic
X improves density	☐ improves efficiency	☐ improves signal to noise ratio
☒ increases operating speed	☐ fewer component parts	☐
☒ improves reliability	☐ reduces cost of manufacturing	☐

Discussion of advantage of the invention over other solutions:
This invention is a new approach to easily optimize the reliability of Cu interconnects in terms of EM and dielectric breakdown. Additionally, this is done with little or no cost in terms of tool throughput.

First written description* of invention, date:	First external disclosure to (name):
Date of first drawing*: Date invention first reduced to practice:	Date of first external disclosure, none ☐ External disclosure under NDA* No ☐ Yes ☐
Made by (name): Tested by (name):	First external disclosure or use by: presentation ☐, announcement ☐, sample ☐, sale ☐, other ☐
Date of first computer simulation:	Date of Non-Disclosure Agreement*, if any:
Date of first successful test:	Date of first publication*:
any of above occurred outside of USA ☐	Publication name:
* *attach copy if possible*	Date of first commercial use:

Does plan exist to publish, disclose or sell? If so, where and when?_____
Was invention conceived, constructed or tested pursuant to the performance under a development contract with another company: No ☐, Yes ☐. If yes, Company name_____
If yes, name of AMD business contact and contract no._____
Was invention jointly developed with participation of inventors from outside AMD: No ☐, Yes ☐.
If yes, Company name_____

I have read and understood this disclosure and read and signed each page of the attachments:

Witness 1 signature: Christine M Esber Date: 4/9/01
Printed name: Christine M Esber Employee #: 80905

Witness 2 signature: E. Todd Ryan Date: 4/9/01
Printed name: E Todd Ryan Employee #: 68767

*After completing to this point, deliver to department reviewer: date delivered*_____

Witness 1 initial: cmr Witness 2 initial: ETR

AMD INVENTION DISCLOSURE

TLD ID#_____ Rec'd date _____
Sunnyvale x42110, return to MS68, Texas x55964 return to MS562

DISCLOSURE EVALUATION (*Entries from this point on are by the Reviewer*)

Does this invention add value to the AMD intellectual property portfolio? Yes ☒ No ☐,
Explain:_____

Do you know of any relevant art? Yes ☐, No ☒ If yes, attach a copy and explain: _____

What application(s) do you foresee for this invention? _____
Advanced Cu – BEOL technology

I estimate the Value* of this invention disclosure is A ☐, B ☒ C ☐, D ☐,
* use worksheet *"Valuing Invention Disclosures and Patents"*.

it **is** ☒, **is not** ☐ recommended to AMD for **U.S. patent application** filing,
it **is** ☒, **is not** ☐ recommended to AMD for **foreign patent application** filing,
it **is** ☐, **is not** ☒ recommended to be held as an AMD **trade secret,**
Give this high priority ☐, **normal** ☒, **low priority** ☐, **in patent application writing.**

GUIDELINES AND CONSIDERATIONS FOR FOREIGN FILING DECISION

Filing foreign patent applications is costly. We should choose to do it only when conditions warrant.
ALL CONDITIONS BELOW MUST APPLY IN ORDER TO INITIATE A FOREIGN FILING:

- ***Invention is High-Valued (A, B)*, and***
- ***Invention is in our technology path (usage), and***
- ***Invention usage is detectable by inspection of product, and***
- ***Invention is relatively hard to design around, and***
- ***Competitor is operating in the country of interest.*** *(see ca000000.xls tabulation of "Factory Sites outside the USA .)*

I recommend filing patent applications in foreign countries checked below:

Japan ☐	S.Korea ☐	Taiwan ☐	U.K. ☐	France ☐	Germany ☒
☐	☐	☐	☐	☐	☐

Reviewer's signature: M. Raab Employee #: 28267 Date: 06-07-01

Reviewer's printed name: M. RAAB

If foreign filing is checked, route to ***Div. VP*** for signature.

VP or Designate approves foreign filing (signature)_____

Reviewer: Complete this page and send (all) disclosures to TLD, including those not recommended for patent application filing.

Nitride Recipes

1.) N-SiN 150 A

Process steps:

1. Set-up
   t = 25 sec ; P = 4,8 Torr ; T = 400 C
   SiH4 = 150 sccm ; NH3 = 260 sccm ; N2 = 8600 sccm
2. Deposition
   t = 3 sec ; P = 4,8 Torr ; T = 400 C ; RF = 520 Watt
   SiH4 = 150 sccm ; NH3 = 260 sccm ; N2 = 8600 sccm
3. Purge
   t = 10 sec ; T = 400 C
   N2 = 8600 sccm
4. Pump
   t = 15 sec , no gas

2. SR-SiN 300 A

Process steps:

1. Set-up
   t = 15 sec ; P = 4,6 Torr ; T = 400 C
   SiH4 = 220 sccm ; NH3 = 50 sccm ; N2 = 7500 sccm
2. Deposition
   t = 6,5 sec ; P = 4,6 Torr ; T = 400 C ; RF = 480 Watt
   SiH4 = 220 sccm ; NH3 = 50 sccm ; N2 = 7500 sccm
3. Purge
   t = 10 sec ; T = 400 C
   N2 = 7500 sccm
4. Pump
   t = 15 sec , no gas

3.) New integrated SiN (N-SiN + SR-SiN)

Process steps:

1. Set-up
   t = 25 sec ; P = 4,8 Torr ; T = 400 C
   SiH4 = 150 sccm ; NH3 = 260 sccm ; N2 = 8600 sccm
2. Deposition
   t = 1,5 sec ; P = 4,8 Torr ; T = 400 C ; RF = 520 Watt
   SiH4 = 150 sccm ; NH3 = 260 sccm ; N2 = 8600 sccm
3. Transition
   t = 5 sec ; P = 4,6 Torr ; T = 400 C
   SiH4 = 220 sccm ; NH3 = 50 sccm ; N2 = 7500 sccm
4. Deposition
   t = 6,5 sec ; P = 4,6 Torr ; T = 400 C ; RF = 480 Watt
   SiH4 = 220 sccm ; NH3 = 50 sccm ; N2 = 7500 sccm
5. Purge
   t = 10 sec ; T = 400 C
   N2 = 8600 sccm
6. Pump
   t = 15 sec , no gas